WHAT IS CLAIMED IS:

1. A nonvolatile semiconductor memory comprising:

a memory cell array formed of a plurality of memory cell strings each connected to a plurality of bitlines;

a plurality of page buffers each connected to a corresponding one of the bitlines;

a plurality of transistors connected between the bitlines and the page buffers, each of the plurality of transistors operative when turned off to electrically isolate each of the plurality of page buffers from the corresponding one of the plurality of bitlines; and

a bitline voltage controller applying a bitline control voltage to gates of the transistors selectively to turn the transistors off thus to effect electrical isolation between each of the plurality of page buffers and the corresponding one of the plurality of bitlines,

wherein the bitline control voltage is charged to a first voltage during a part of a first bitline setup period, a second voltage during the remaining of the first bit line period, and a third voltage during a second bitline setup period.

2. The nonvolatile semiconductor memory of claim 1, wherein the third voltage is lower than the first voltage and higher than the second voltage.

3. The nonvolatile semiconductor memory of claim 2, wherein the first and second voltages are a pass voltage and a ground voltage.

4. The nonvolatile semiconductor memory of claim 2, wherein the third voltage corresponds to the sum of a field inhibition voltage and a threshold voltage of an NMOS transistor, the field inhibition voltage being a minimum source-bulk voltage needed to turn off a parasitic MOS transistor.

5. The nonvolatile semiconductor memory of claim 1, wherein the third voltage is maintained during a program period following the second bitline setup period.

6. The nonvolatile semiconductor memory of claim 5, wherein the bitline control voltage is charged to a fourth voltage during a recovery period following the program period.

7. The nonvolatile semiconductor memory of claim 6, wherein the fourth voltage is a power supply voltage.

8. The nonvolatile semiconductor memory of claim 6, wherein the bitline voltage controller comprises:

a first voltage generator configured to supply the first voltage (VPASS) to a voltage line for transferring the bitline control voltage in response to a first bitline control signal (BLCE1);

a second voltage generator configured to generate the second voltage (GND) at an internal node in response to a second and a third bitline control signal (BLCE2, BLCE3);

a third voltage generator configured to generate the third voltage (Vfi') at the internal node in response to the fourth bitline control signal (BLCE4); and

a switch circuit configured to connect the internal node to the voltage line in response to the second bitline control signal (BLCE2).

9. The nonvolatile semiconductor memory of claim 8, wherein the bitline voltage controller further comprises a discharge circuit configured to discharge a voltage of the voltage line in response to the first and second bitline control signals (BLCE1, BLCE2).

10. The nonvolatile semiconductor memory of claim 8, wherein the bitline voltage controller further comprises a fourth voltage generator configured to generate the fourth voltage in response to the third control signal.

11. The nonvolatile semiconductor memory of claim 8, wherein the first control signal is activated during the part of the first bitline setup period.

12. The nonvolatile semiconductor memory of claim 8, wherein the second control signal is activated during the remaining of the first bitline setup period , the second bit line setup period, the program period and the recovery period.

13. The nonvolatile semiconductor memory of claim 8, wherein the third control signal is activated during the remaining of the first bitline setup period, the second bitline setup period and the program period.

14. The nonvolatile semiconductor memory of claim 8, wherein the fourth control signal is activated during the second bitline setup period and the program period.

15. The nonvolatile semiconductor memory of claim 8, wherein the first voltage generator includes a level shifter and the fourth voltage generator includes a comparator and a voltage divider, respectively.

16. A method of programming in a nonvolatile semiconductor memory which has a plurality of memory cell strings connected to a plurality of bitlines and constructed of a plurality of memory cell transistors whose gates are coupled to a plurality of wordlines, and a plurality of registers corresponding to the bitlines, the method comprising the steps of:

applying a first voltage to a first one of the bitlines and a second voltage to a second one of the bitlines during a part of the first bitline setup period, the first bitline being adjacent to the second bitline, the first and second voltages being supplied from the registers;

electrically isolating the first and second bitlines from their corresponding registers during the remaining of the first bitline setup period;

charging the first bitline up to a third voltage higher than the first voltage and lower than the second voltage during a second bitline setup period following the first setup period; and

applying a fourth voltage to a wordline after substantially inhibiting current into the first and second bitlines during a program period, wherein the third voltage to the first bitline is maintained during the program period.

17. The method of claim 16, wherein the first, second, third and fourth voltages are a ground voltage, a power supply voltage, an inhibit voltage and a program voltage.

18. The method of claim 16, wherein the nonvolatile semiconductor memory further comprises a plurality of transistors connected between the bitlines and the registers; and a bitline voltage controller configured to apply a bitline control voltage to gates of the transistors.

19. The method of claim 18, wherein the bitline control voltage is charged to a fifth voltage (VPASS) during the part of the first bitline setup period, the first voltage during the remaining of the first bit line setup period, a sixth voltage during the second bitline setup

period and a program period following the second bitline setup period, the sixth voltage being lower than the fifth voltage and higher than the first voltage.

20. The method of claim 19, wherein the fifth voltage is a pass voltage.

21. The method of claim 19, wherein the sixth voltage corresponds to the sum of the third voltage and a threshold voltage of an NMOS transistor, the third voltage being a minimum source-bulk voltage needed to turn off a parasitic MOS transistor.

22. The method of claim 19, wherein the bitline control voltage is charged to the second voltage (VCC) during a recovery period following the program period.

23. The method of claim 19, wherein the bitline voltage controller comprises:

a first voltage generator configured to supply the fifth voltage (VPASS) to a voltage line for transferring the bitline control voltage in response to a first bitline control signal (BLCE1);

a second voltage generator configured to generate the first voltage (GND) at an internal node in response to a second and a third bitline control signal (BLCE2,BLCE3);

a third voltage generator configured to generate the sixth voltage (Vfi') at the internal node in response to the fourth bitline control signal (BLCE4); and

a switch circuit configured to connect the internal node to the voltage line in response to a second bitline control signal (BLCE2).

24. The method of claim 23, wherein the bitline voltage controller further comprises a discharge circuit configured to discharge a voltage of the voltage line in response to the first and second bitline control signals (BLCE1,BLCE2).

25. The method of claim 23, wherein the bitline voltage controller further comprises a fourth voltage generator configured to generate the second voltage in response to the third bitline control signal.

26. The method of claim 23, wherein the first bitline control signal is activated during the part of the first bitline setup period.

27. The method of claim 23, wherein the second bitline control signal is activated during the remaining of the first bitline setup period, the second bitline setup period, the program period and the recovery period.

28. The method of claim 23, wherein the third control signal is activated during the remaining of the first bitline setup period, the second bitline setup period and the program period.

29. The method of claim 23, wherein the fourth control signal is activated during the second bitline setup period and the program period.

30. The method of claim 23, wherein the first voltage generator includes a level shifter.

31. The method of claim 16, wherein the nonvolatile semiconductor memory further comprises a plurality of load transistors configured to supply current to the bitlines in response to a load control voltage.

32. The method of claim 31, wherein the load control voltage is charged to the second voltage during the first bitline setup period, a fifth voltage (Vload) during the remaining of the second bitline setup period, and the second voltage during a program period following the second bitline setup period, the fifth voltage being higher than the first voltage and lower than the second voltage.